Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Circuits & Electronics
Fall 2006

Quiz #1

3 October 2006

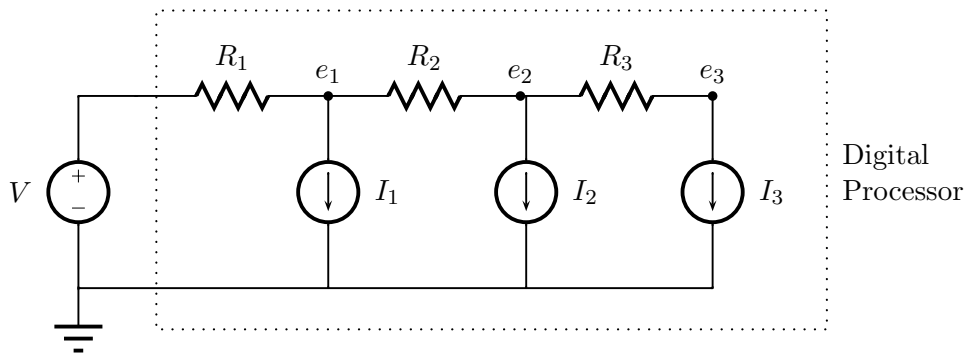
Name: _____

- There are 14 pages in this exam, including this cover page.
- Please put your name in the space provided above, and circle the name of your recitation instructor together with the time of your recitation.
- Do your work for each question within the boundaries of that question, or on the back of the preceding page. When finished, write your answer to each question in the corresponding answer box that follows the question.
- Remember to include the sign and units for all numerical answers.
- This is a closed-book exam, but calculators are allowed.
- You have 2 hours to complete this exam.
- Good luck!

Problem 1	Problem 2	Problem 3	Total Grade

Problem 1 – 35 Points

The circuit shown below models the power distribution network in a digital processor. The voltage source models the external supply that powers the processor, the resistors model the power distribution wiring internal to the processor, and the current sources model the loads presented by the individual parts of the processor. The source values V, I_1, I_2 and I_3 are all positive, as are the three internal node voltages e_1, e_2 and e_3. Further, depending upon whether the corresponding part of the processor is in use or not, I_1, I_2 and I_3 can each take on only the value of either I or zero.



(1A) (10 Points) Using the node method, develop a set of simultaneous equations for the power distribution network that can be solved for the three unknown node voltages e_1, e_2 and e_3. Express these equations in the form

$$G \begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix} = S$$

where G is a 3×3 matrix of conductance terms and S is a 3×1 vector of terms involving the sources V, I_1, I_2 and I_3. *You need not solve the set of equations for the node voltages.*

Answer

(1B) (10 Points) Given the possible values for I_1, I_2 and I_3, what are the maximum and minimum values that e_2 can exhibit? Express your answer in terms of V, I, R_1, R_2 and R_3.

Max $e_2 =$	Min $e_2 =$

(1C) (5 Points) Given the possible values for I_1, I_2 and I_3, what is the maximum power that the voltage source must be able to supply to the processor? Express your answer in terms of V, I, R_1, R_2 and R_3.

Max Power =

(1D) (5 Points) If any node voltage inside the processor power distribution network falls below a threshold value e_{Min}, then the part of the processor connected directly to that node will fail to operate properly. Given the possible values for I_1, I_2 and I_3, what is the minimum value for V that guarantees that all parts of the processor will always operate properly? That is, what is the minimum value of V required to guarantee that e_1, e_2 and e_3 never fall below e_{Min}? Express your answer in terms of I, R_1, R_2, R_3 and e_{Min}.

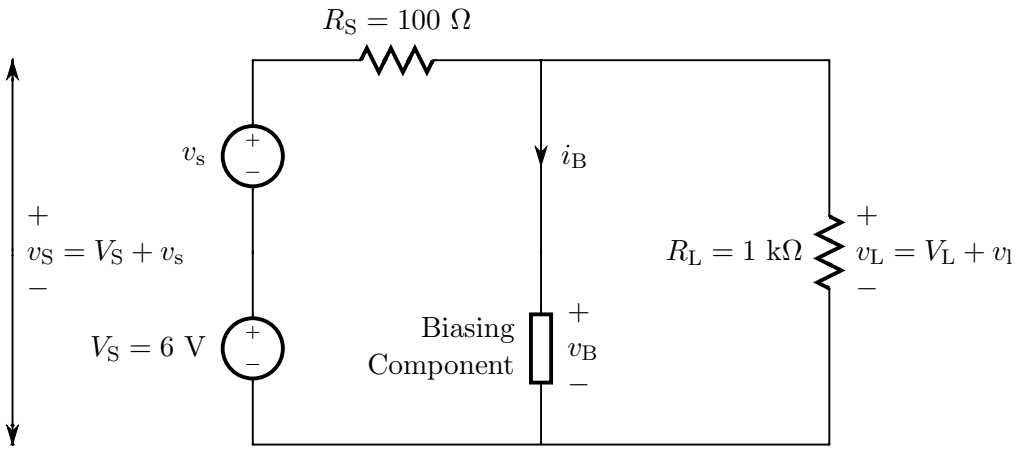
Min V =

(1E) (5 Points) If any node voltage inside the processor rises above a threshold value e_{Max}, then the part of the processor connected directly to that node will be damaged. Given the possible values for I_1, I_2 and I_3, what is the maximum value for V that guarantees that no part of the processor will be damaged? That is, what is the maximum value of V required to guarantee that e_1, e_2 and e_3 never exceed e_{Max}? Express your answer in terms of I, R_1, R_2, R_3 and e_{Max}.

Max V =

Problem 2 – 35 Points

A noisy power supply with total Thevenin voltage v_S and Thevenin resistance R_S is connected to a load that is modeled by the resistor R_L as shown below. A biasing component, which could be linear resistor or a nonlinear component, is placed in parallel with the power supply and load. It will be used to adjust the load voltage v_L. The noise in the power supply is modeled by the small signal v_s superimposed on the constant supply voltage V_S. Thus, V_S and v_s are the large-signal and small-signal components of the total power supply voltage v_S, respectively. Correspondingly, V_L and v_l are the large-signal and small-signal components of the total load voltage v_L, respectively, as indicated below. The noise v_s satisfies $v_s \ll V_S$, and is responsible for the presence of v_l in v_L.



For Parts (2A) and (2B), let the biasing component be a linear resistor having resistance R_B.

(2A) (5 Points) In the absence of any power supply noise voltage, that is, for $v_s = 0$ V, determine a numerical value for R_B so that $V_L = 5$ V. *Remember to provide units!*

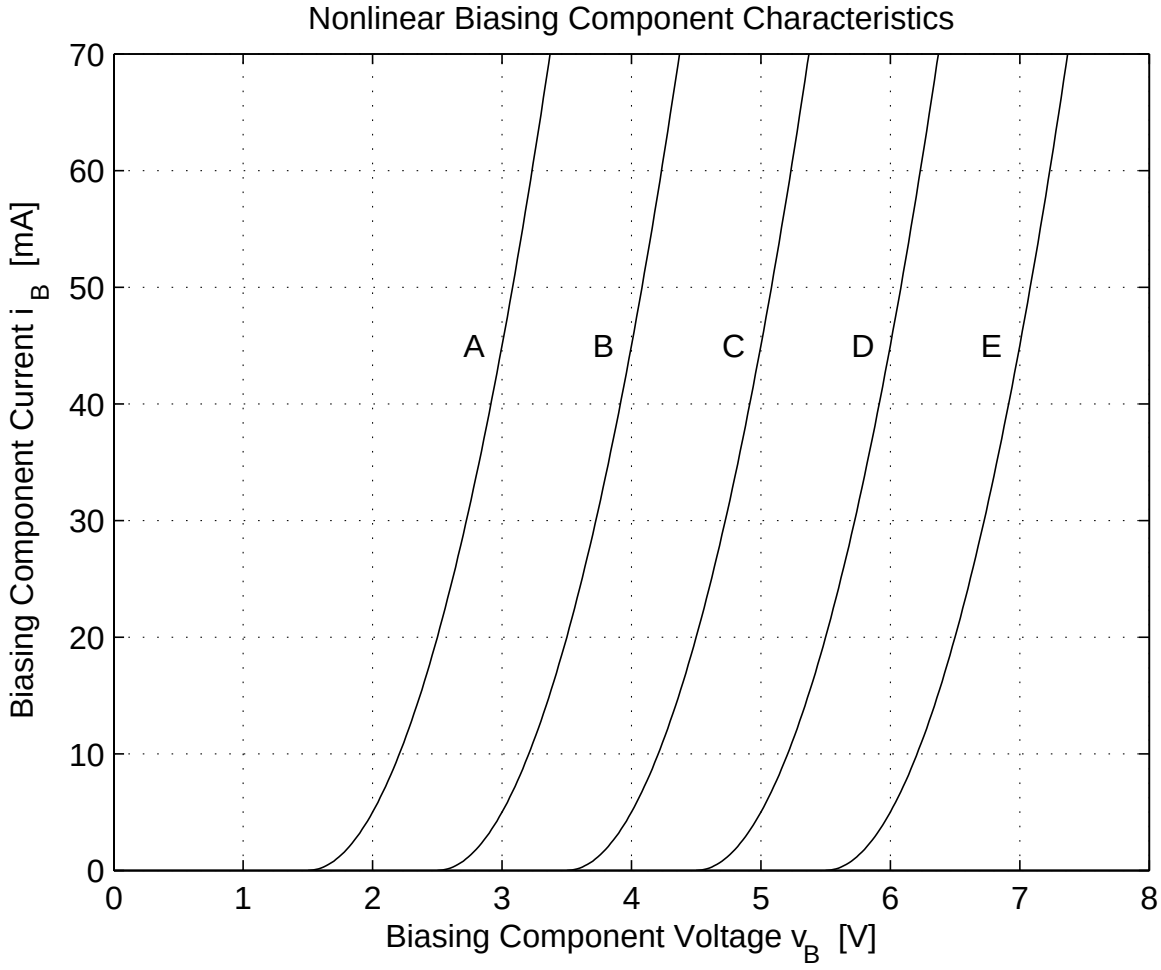
$R_B =$

(2B) (5 Points) Now let v_s be non-zero. For the conditions of Part (2A), determine the ratio v_l/v_s. *Numerical answer expected.*

$v_l/v_s =$

For Parts (2C) and (2D), let the biasing component be a nonlinear component having the characteristic given by $i_B = 20$ mA $\times$ $((v_B - V_X)$ / $(1$ V$))^2$ for $v_B \geq V_X$, and zero otherwise. Here, V_X is the voltage at which the characteristic intersects the horizontal axis.

(2C) (10 Points) The characteristics of five nonlinear components are shown in the graph below. The corresponding V_X is 1.5 V, 2.5 V, 3.5 V, 4.5 V and 5.5 V, for characteristics A through E, respectively. Which nonlinear component should be used so that $V_L = 5$ V in the absence of any power supply noise? Also give a reason. *(No credit without a reason.)*



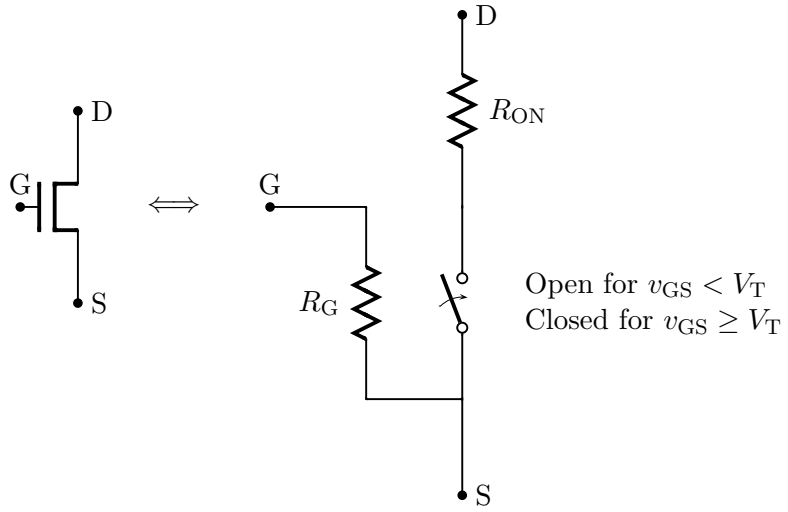
Circle One: A B C D E

(2D) (15 Points) Again let v_s be non-zero. For the conditions of Part (2C), approximate the ratio v_l/v_s. You may use either a graphical or an analytic method. Hint: your answer should be smaller than that found in Part (2B), demonstrating an important use of nonlinear components. *Numerical answer expected.*

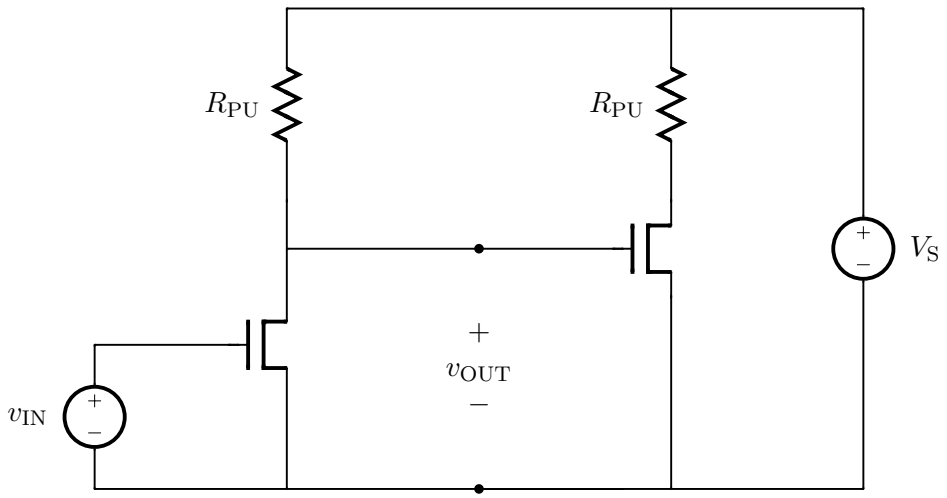
$v_l/v_s =$

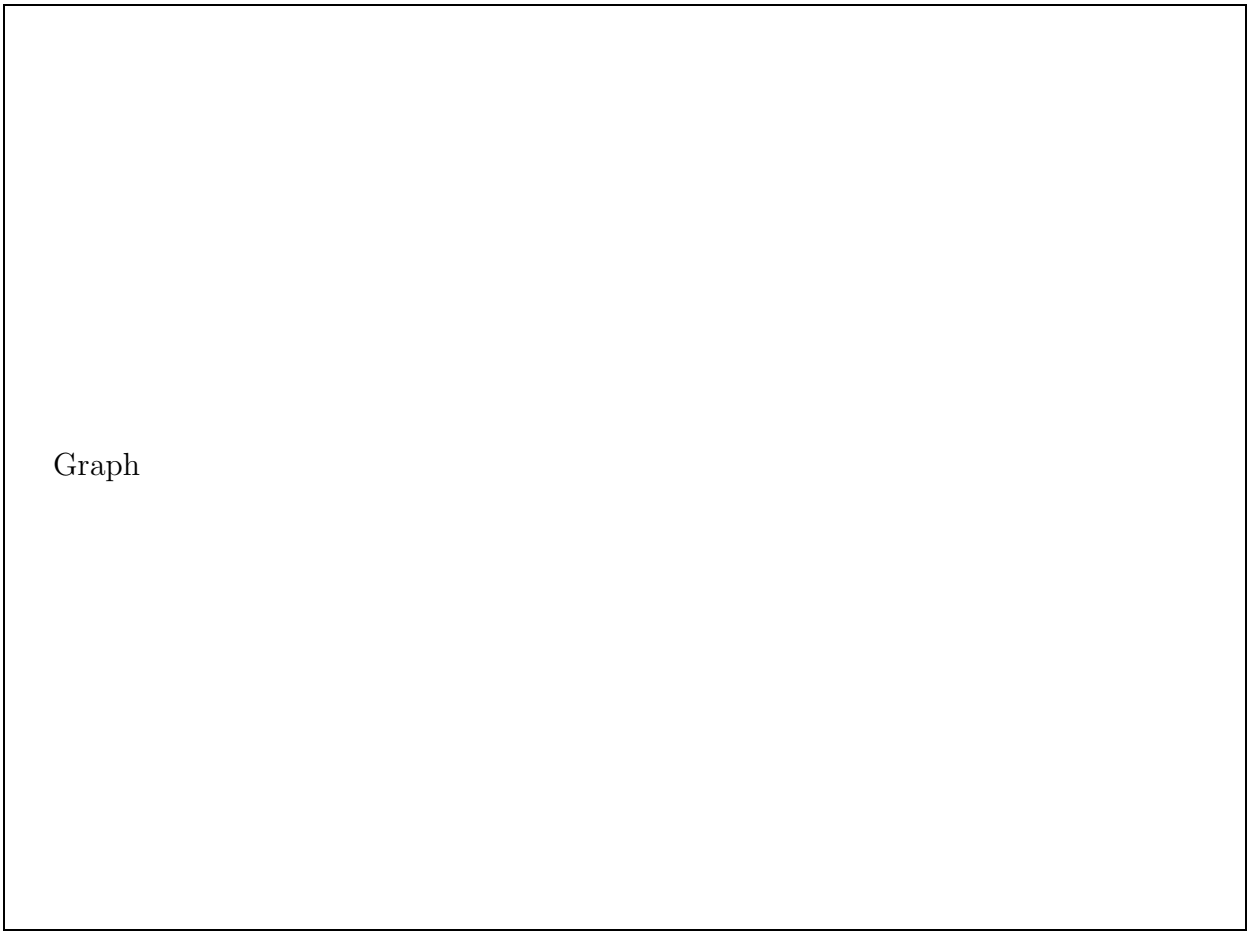
Problem 3 – 30 Points

In this problem the switch-resistor model of the MOSFET is expanded to include a finite gate-source resistance R_G. The corresponding model for the MOSFET is shown below.

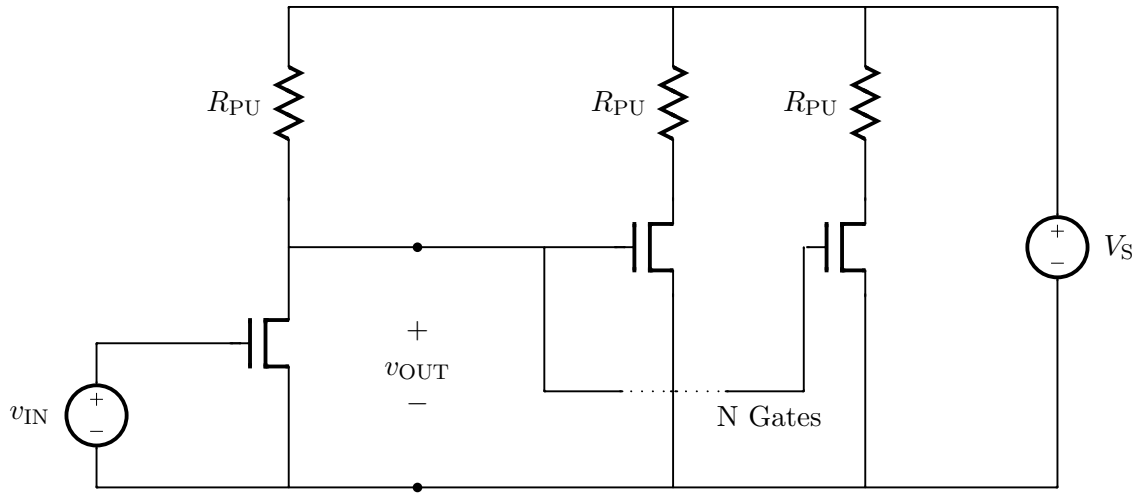


(3A) (15 Points) Two inverters are connected in series as shown below. The MOSFET in both inverters has a finite gate-source resistance as modeled above. For this circuit, sketch and clearly label the transfer function for the first inverter, that is, v_{OUT} as a function of v_{IN}, over the range $0 \leq v_{IN} \leq V_S$ in the space given below. Assume that $V_S > V_T$.





(3B) (15 Points) Now consider the case in which the output of the first inverter is connected to the input of N identical inverters as shown below. Assuming that $V_{\rm T}$, $R_{\rm ON}$ and $R_{\rm G}$ are all given, over what range must $R_{\rm PU}$ be designed so that the first inverter can successfully switch the states of the successive inverters. That is, over what range must $R_{\rm PU}$ be designed so that $v_{\rm OUT} > V_{\rm T}$ when $v_{\rm IN} < V_{\rm T}$, and $v_{\rm OUT} < V_{\rm T}$ when $v_{\rm IN} > V_{\rm T}$. Again assume that $V_{\rm S} > V_{\rm T}$.



$< R_{\rm PU} <$